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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,811	12/15/2003	Tadanori Nishikobara	03752/LH	5405

1933 7590 05/02/2005

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EXAMINER	
LE, JOHN H	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,811	NISHIKOBARA ET AL.	
	Examiner	Art Unit	
	John H. Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,11-18 and 23* is/are rejected.

7)☒ Claim(s) *7-10 and 19-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/15/03, 04/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 11-16, and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Agilent Technologies ("Frequency Agile Jitter Measurement System", August 22, 2002).

Regarding claims 1 and 13, Agilent teaches a pattern dependent jitter measuring apparatus comprising: a clock generating unit (83752A) which generates a clock signal having a predetermined frequency (e.g. Fig.9, page 6, Cols.1-2); and a pattern generating unit (71612C) which outputs a data signal having a predetermined pattern in which one frame is configured from a predetermined bit length, so as to be synchronized with the clock signal outputted from the clock signal generating unit (e.g. Fig.9, Page 7, Cols.1-3), wherein the pattern dependent jitter measuring apparatus further comprises: a waveform information acquiring unit (sampling oscilloscope) which receives the data signal outputted from the pattern generating unit as a data signal to be measured, and receives the clock signal outputted from the clock generating unit, and which acquires information of waveform in the same time domain of the data signal to be measured and the clock signal (e.g. Figs. 9, 23, Page 12); an averaging processing unit (intermediate frequency unit (IF)) which carries out averaging processing on the

waveform acquired by the waveform information acquiring unit (e.g. Figs. 9, 23, Page 12); a phase difference detecting unit determining the per-bit phase difference between the data signal to be measured and the clock signal, based on the waveform information averaged by the averaging processing unit (e.g. Fig.8, Page 6, Col.3); a frequency band limiting processing unit (band pass filter) which carries out predetermined frequency band limiting processing on information of the per-bit phase difference obtained by the phase difference detecting unit (e.g. Fig.8, Page 6, Col.3, Page 11, Col.3); and a measured result outputting unit which outputs the phase difference information on which the frequency band limiting processing is carried out by the frequency band limiting processing unit, as pattern dependent jitter (e.g. Figs.8-9, Pages 6-7).

Regarding claims 2 and 14, Agilent teaches the pattern generating unit is configured to include a data signal in which an unscrambled specific pattern exists at a head position of each frame, as the data signal outputted from the pattern generating unit (e.g. Fig.9).

Regarding claims 3 and 15, Agilent teaches the waveform information acquiring unit (sampling oscilloscope) is configured to receive a data signal to be outputted by a measuring object which has received the data signal outputted from the pattern generating unit, as the data signal to be measured, and receive a clock signal outputted from the clock generating unit, and acquire waveform information in the same time domain of the data signal to be measured and the clock signal (e.g. Figs. 9, 23).

Regarding claims 4 and 16, Agilent teaches the measuring object includes equipment configured such that, when pattern dependent jitter is included in a data signal to be inputted, a pattern dependent jitter component included in the inputted data signal can be removed by waveform shaping processing at the inside thereof, and a data signal including random noise jitter and pattern dependent jitter which the measuring object itself internally generates is outputted to the waveform information acquiring unit as the data signal to be measured (e.g. Pages 13-14).

Regarding claim 23, Agilent teaches the acquiring of the waveform information and the averaging processing are carried out by a sampling oscilloscope (e.g. Figs. 9, 23, Page 12).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5-6 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agilent Technologies ("Frequency Agile Jitter Measurement System", August 22, 2002) in view of Agilent Technologies ("Jitter Separation using the Agilent 86100C Infiniium DCA-J", December 09, 2003).

Regarding claims 5-6 and 17-18, Agilent ("Frequency Agile Jitter") fails to teach the pattern generating unit is configured to output a frame synchronization signal synchronized with data output timing at an arbitrary bit position in one frame of the data

signal, to the waveform information acquiring unit, and the waveform information acquiring unit is configured to acquire a predetermined number of frames of the waveform information of the data signal to be measured and the clock signal by using the timing when the frame synchronization signal is inputted as a standard timing, wherein the averaging processing unit is configured to determine one frame of waveform information of the clock signal and the data signal to be measured from each of which the random noise jitter component has been removed, by averaging the predetermined number of frames of waveform information which are acquired by the waveform information acquiring unit.

Agilent ("Jitter Separation") teaches the pattern generating unit is configured to output a frame synchronization signal synchronized with data output timing at an arbitrary bit position in one frame of the data signal, to the waveform information acquiring unit, and the waveform information acquiring unit is configured to acquire a predetermined number of frames of the waveform information of the data signal to be measured and the clock signal by using the timing when the frame synchronization signal is inputted as a standard timing, wherein the averaging processing unit is configured to determine one frame of waveform information of the clock signal and the data signal to be measured from each of which the random noise jitter component has been removed, by averaging the predetermined number of frames of waveform information which are acquired by the waveform information acquiring unit (e.g. Agilent "Jitter Separation", Page 10, 15-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the pattern generating unit is configured to output a frame synchronization signal synchronized with data output timing at an arbitrary bit position in one frame of the data signal as taught by Agilent ("Jitter Separation") in a pattern dependent jitter measuring apparatus of Agilent ("Frequency Agile Jitter") for the purpose of providing a perform jitter separation (Agilent "Jitter Separation", Page 1).

Allowable Subject Matter

5. Claims 7-10, 19-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

In combination with other limitations of the claims, the cited prior arts fails to teach the phase difference detecting unit is configured such that a phase difference (time difference) $\Delta T(i)$ between level displacement timing of the clock signal which is determined by the averaging processing unit, and from which the random noise jitter component has been removed, and a code boundary of the data signal to be measured, is determined for each bit, and such that per-bit phase difference $\Delta T(i)'$ is determined by

$\Delta T(1)' = 0$, and

$\Delta T(i)' = \Delta T(i) - \Delta T(1)$ $(I = 2, 3, \ldots, N)$,

by correcting the phase differences $\Delta T(2)$, $\Delta T(3)$,..., $\Delta T(N)$ from the second bit on by the bit difference $\Delta T(1)$ of the first bit, as recited in (amended) claim(s) 7 and 19.

Other Prior Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Koishi et al. (USP 5,463,639) disclose an automatic pattern synchronizing circuit re-times the phase differences between clocks, thereby adjusting test pattern outputs from a device under test. The automatic pattern synchronizing circuit includes a reference voltage generator for providing a threshold voltage, a comparator for converting an input signal into a rectangular signal, a flip-flop, a pattern-counter part for counting a signal from the flip-flop and a control part for setting the threshold voltage in the comparator. The automatic pattern synchronizing circuit automatically synchronizes voltage patterns. In particular, the high and low voltage levels of the input waveform are automatically measured and the optimum threshold voltage is automatically set.

West (US 6,622,107) discloses edge placement and jitter measurement for electronic elements

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John H Le whose telephone number is 571-272-2275. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John H. Le

Patent Examiner-Group 2863

April 25, 2005

MICHAEL NGHIEM
PRIMARY EXAMINER